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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/161,405	09/28/1998	HIRAKU KOZUKA	862.2480	7603

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EXAMINER	
WHIPKEY, JASON T	

ART UNIT	PAPER NUMBER
2612	55

DATE MAILED: 07/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/161,405	KOZUKA, HIRAKU	
	Examiner	Art Unit	
	Jason T. Whipkey	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8,11,14 and 33-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8,11,14,33-35,37 and 38* is/are rejected.

7)☒ Claim(s) *36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 3, 2004, has been entered.

Response to Arguments

2. Applicant's arguments with respect to claims 33 and 38 have been considered but are moot in view of the new ground of rejection.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 8, 11, 14, and 33-38 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the

relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

Claim 33 has been amended to now recite "a plurality of photo sensor chips mounted on a single mounting substrate, each photo sensor chip having a plurality of photo-electric conversion circuits ... wherein each said photo-electric conversion circuit has a photo-electric conversion part and an amplifier for amplifying an output signal from the photo-electric conversion part". In reconciling the claim with Figure 3, one can conclude that part 300 corresponds to "a single mounting substrate" and parts 100, 100', etc., correspond to "a plurality of photosensor chips". Figure 4A shows photosensor chip 100 in detail. One can conclude that part 10 corresponds to "a photo-electric conversion part", since a plurality of parts 10 are included on each chip. However, each part 10 does *not* have an associated amplifier. Instead, each chip 100 has amplifiers 11 and 12, which are shared among all sensor elements 10.

Claim 38 uses similar language.

Claims 8, 11, 14, and 34-37 are rejected because they are dependent on claims 33 and 38.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 33-35, 37, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura (U.S. Patent No. 5,321,528) in view of Kondou (U.S. Patent No. 5,021,888) and further in view of Ansari (U.S. Patent No. 6,288,742) and Akimoto (U.S. Patent No. 4,942,474).

Regarding claims 33 and 38, Nakamura discloses an image sensor consisting of multiple sensor chips that are "aligned" (column 2, line 66, through column 3, line 4), indicating they are mounted on a base ("a single mounting substrate"). Each chip — 1-1 in Figure 1, for example — has an unlabeled output bus connecting the drains of transistors 6-1-1, 6-1-2, etc., which are connected to photoconversion cells 2-1-1, 2-1-2, etc. ("a photo-electric conversion part"). MOS switch 10-1 ("a photo sensor chip output device") outputs signals from the common output line connected to the output of amplifier 9-1 to the output of chip 1-1.

The output bus in each chip is used to output light signal voltage V2 (column 3, lines 52-55) and noise signal voltage V1 (column 3, lines 36-41). An amplifier circuit ("a correction circuit"), consisting of parts 33-39 shown in Figure 3, receives the output of an inter-chip bus. Buffer amplifier 33 receives both the noise signal V1 (column 4, lines 3-8) and the light signal V2 (column 4, lines 16-20) from the bus. Capacitor 35 receives these signals and finds the difference (column 4, lines 16-30). Components 33-39 comprise a correction circuit 140 (column 5, lines 11-16), and correction circuit 140 is part of a printed circuit board (column 5, lines 56-58).

Nakamura is silent with regard to including a noise reduction circuit on the base with the sensor chips.

Kondou discloses an imaging device (Figure 1) where flexible printed circuit board 11 is attached to solid state imaging element 10 (column 3, lines 29-31). Included on flexible printed

circuit board 11 is a plurality of components 13, including a noise reduction circuit (column 3, lines 32-35).

An advantage to including a noise reduction circuit on a printed circuit board with an imaging device is that a strong, dependable, permanent connection can be made between the imager and the noise reduction circuit, which makes the chance of noise resulting from a poor connection less likely. For this reason, it would have been obvious at the time of invention to have Nakamura include his noise-reducing buffer amplifier on the same board as the image sensor.

Nakamura and Kondou are silent with regard to using one noise reduction circuit to process signals from a plurality of image sensing devices.

Ansari discloses a video camera with multiple image sensors. Figure 2C shows that a common correlated double sampling circuit 6 can be used to process signals from each of the two CCDs 5 (column 3, line 66, through column 4, line 15). Correlated double sampling circuits inherently compensate for the unevenness of noise signals between pixels (i.e., they cancel noise specific to a pixel).

As stated in column 3, lines 63-66, an advantage to using one CDS circuit is that the cost of the system can be reduced. For this reason, it would have been obvious at the time of invention to have Nakamura's and Kondou's system use a single noise-correction circuit with a plurality of image sensors.

Nakamura is also silent with regard to including an output terminal connected to the output of the noise-reducing buffer amplifier.

Kondou shows in Figure 1 that connection pads 15 have extension cables 16 connected to them, wherein connection pads 15 are also connected to the output of components 13 (column 3, lines 35-37).

An advantage to including output terminals on a mounting board is that a connection may be made to a card slot or wiring at a location that requires the least disturbance of the components on the board. This prevents components from being damaged. For this reason, it would have been obvious at the time of invention to have Nakamura include output connections on the outside of his mounting board.

Nakamura is also silent with regard to including an amplifier with each photo-electric conversion part, wherein the amplifier outputs a noise offset signal that is to be removed.

Akimoto discloses an image sensor, as shown in Figure 3. Each pixel ("a photo-electric conversion circuit") includes a photodiode 1 ("a photo-electric conversion part") and an amplifier 4 (column 2, lines 60-61). A reset operation is performed by reset switch 3, which causes amplifier 4 to reset and output a noise signal that includes its offset (column 3, lines 6-24). This noise signal is subtracted from the image signal to reduce noise (column 3, lines 20-24).

An advantage to including an amplifier in each pixel is that noise is reduced, as compared to column amplifiers or whole-sensor amplifiers. An advantage to resetting the amplifier to obtain its offset noise is that the noise measurement is more accurate. For these reasons, it would have been obvious at the time of invention to have Nakamura's imaging system include an amplifier in each pixel, wherein the amplifier's offset noise can be measured by resetting it.

Regarding claim 34, Nakamura discloses a differential circuit (capacitor 35) as described above. Additionally, capacitor 35 is part of a clamping circuit consisting of parts 35-38. The

clamping circuit clamps the signal using clamping voltage VC from clamped voltage source 38 (column 4, lines 11-12).

Regarding claim 35, the chip is reset via reset terminal 24 (column 3, lines 39-40). After the inter-chip bus is reset, clamping circuit 35-38 clamps the reset state (column 4, lines 5-12).

Regarding claim 37, Nakamura shows that capacitor 35 is part of a clamping circuit consisting of parts 35-38. The clamping circuit clamps the signal using clamping voltage VC from clamped voltage source 38 (column 4, lines 11-12).

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Kondou and further in view of Ansari, Akimoto, and Surisawa (U.S. Patent No. 6,215,521).

Claim 8 may be treated like claim 33. However, Nakamura is silent with regard to using a power supply voltage with the photosensor chips that is lower than the power supply voltage supplied to the processing means.

Surisawa discloses an image sensor on a substrate 1 (Figure 10A). The voltage V_{sub} supplied to the substrate is larger than the voltage V_D supplied to the image sensor (column 13, lines 6-8). The advantage to having separate power supplies is that the appropriate voltage may be supplied to each component without excess, which saves power. For this reason, it would have been obvious to have separate power supplies for the chips and the substrate.

8. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Kondou and further in view of Ansari, Akimoto, and Hamasaki.

Claim 11 may be treated like claim 33. However, Nakamura is silent with regard to isolating the ground wiring for the photosensor chips and the processing circuitry.

Hamasaki discloses an image pickup device on a substrate 72 (Figure 4). Output section 78 is also included on substrate 72. Grounding wiring 80 grounds the imaging area (column 6, lines 33-42). Grounding wiring 88 grounds output section 78 (column 6, lines 51-56). As stated in column 6, line 68, through column 7, line 7, this prevents output section 78 from affecting the sensing section. For this reason, it would have been obvious for Nakamura's system to include separate ground wiring for the photosensor chips and the processing circuitry.

9. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Kondou and further in view of Ansari, Akimoto, Surisawa, and Hamasaki.

Claim 14 may be treated like claim 8. However, Nakamura is silent with regard to isolating the ground wiring for the photosensor chips and the processing circuitry.

Hamasaki discloses an image pickup device on a substrate 72 (Figure 4). Output section 78 is also included on substrate 72. Grounding wiring 80 grounds the imaging area (column 6, lines 33-42). Grounding wiring 88 grounds output section 78 (column 6, lines 51-56). As stated in column 6, line 68, through column 7, line 7, this prevents output section 78 from affecting the sensing section. For this reason, it would have been obvious for Nakamura's system to include separate ground wiring for the photosensor chips and the processing circuitry.

Allowable Subject Matter

10. Claim 36 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

No prior art could be located that teaches or fairly suggests a noise compensation circuit with a plurality of serially connected clamp circuits connected to the output of an image sensor.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason T. Whipkey, whose telephone number is (703) 305-1819. The examiner can normally be reached Monday through Friday from 8:30 A.M. to 6:00 P.M. eastern daylight time, alternating Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R. Garber, can be reached on (703) 305-4929. The fax phone number for the organization where this application is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JTW
June 28, 2004

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